UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,723	11/13/2002	Kevin A. Batson	FIS920010179	6157

30449 7590 09/20/2005

SCHMEISER, OLSEN + WATTS
3 LEAR JET LANE
SUITE 201
LATHAM, NY 12110

EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,723	BATSON ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,319,589 to Yamagata *et al* (hereafter Yamagata) in view of U.S. Patent No. 5,134,585 to Murakami *et al* (hereafter Murakami).

Yamagata discloses a content-addressable memory with bitline replacement that uses a non-adjacent spare adjacent bitline. Referring to Fig. 16 of Yamagata, a "coupling circuit" 10 for coupling to bitlines, through connection lines (DT0-DT35, DTS), and their complements, to data lines (IO0-IO35) is controlled by a "steering signal" (400-435) for each data line. Yamagata's "coupling circuit", in operation, "couples (to) a first respective bitline or to a second respective bitline based on a steering signal", however Yamagata's "first bitline" and the replacement "second bitline" (DTS) are non-adjacent, except in the case of one bitline (DT_0). Yamagata further shows a circuit (500-535, 5S) that "maintains said first respective bitline at a desired potential after said data line is coupled to said second bitline" so that a faulty unselected bitline does not introduce noise in reading. Yamagata's bitline coupling selection signals (NED) are controlled (Fig. 18) by a combination of fuse (46) and latch (47), thereby providing "fuse latches".

Murakami discloses a memory array with bitline replacement using adjacent bitlines (Fig. 8), which is a well-known functional equivalent alternative to using a non-adjacent spare bitline for bitline replacement.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Yamagata's memory chip by replacing the non-adjacent bitline sparing with adjacent bitline sparing. Such a substitution would have been obvious because Murakami's adjacent bitline sparing was already a well-known functional equivalent alternative to non-adjacent bitline sparing.

Regarding claims 4 and 13, for inverted bitlines (DT/0-DT/35), the "desired potential is ground".

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,714,430 to Srinivasan *et al* (hereafter Srinivasan) in view of U.S. Patent No. 5,319,589 to Yamagata *et al* (hereafter Yamagata).

Srinivasan discloses a content-addressable memory (CAM) with one or more spare columns (*i.e.* spare "bitlines"). As shown in FIGs. 9A and 9B, coupling circuitry (902, 904) is provided by MUXes under control of steering circuitry (specification, col. 11 line 10 to col. 12 line 44). Further sown are bitlines (COL0-COLx, Spare Column) and data lines (D[0]-D-{x]) provided in an arrangement wherein the coupling circuitry "couples each respective data line to a first respective bitline or a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline." Srinivasan does not disclose "a circuit that maintains said first

respective bitline at a desired potential after said data line is coupled to said second bitline."

Yamagata discloses a CAM with a spare column. Yamagata teaches providing a circuit (500-535, 5S) that maintains a replaced bitline at a desired potential so that the replaced bitline doesn't introduce noise in reading.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate Yamagata's replaced bitline potential-maintaining feature into Srinivasan's bitline replacement. Such incorporation would have been obvious because Yamagata teaches that a replaced bitline potential-maintaining feature has an advantage of preventing the replaced bitline from introducing noise in reading.

Response to Arguments

4. Applicant's arguments filed 05 July 2005 have been fully considered but they are not persuasive.

The standing rejection does not require replacing the switching network of Yamagata with the switching network of Murakami, but instead substitutes non-adjacent bitline sparing with adjacent bitline sparing. Such a substitution is trivially simple to perform, and merely involves changing the connections to the switches SW0-SW35 such that the lower position on each switch couples to the adjacent amplifier (901, in the case of SW0, etc.) instead of to the spare amplifier.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb